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TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No: SEC.506

In Re Application Of: **Byoung-Taek LEE et al.**

Serial No.	Filing Date	Examiner	Group Art Unit
09/276,803	26 March 1999	Neal BEREZNY	2823

Invention: **METHOD FOR MANUFACTURING CAPACITOR OF SEMICONDUCTOR DEVICE HAVING DIELECTRIC LAYER OF HIGH DIELECTRIC CONSTANT**

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **29 December 2003**

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Signature

Dated: **27 February 2004**

KENNETH D. SPRINGER
REG. NO.: 39,843

VOLENTINE FRANCOS, PLLC
12200 SUNRISE VALLEY DRIVE, SUITE 150
RESTON, VA 20191

TEL. NO.: (703) 715-0870

cc:

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of:

Byoung-taek LEE et al.

Group Art Unit: 2823

Serial No.: 09/276,803

Examiner: Neal BEREZNY

Filed: 26 March 1999

METHOD FOR MANUFACTURING CAPACITOR OF SEMICONDUCTOR DEVICE HAVING DIELECTRIC LAYER OF HIGH DIELECTRIC CONSTANT

APPEAL BRIEF

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Sir:

In response to the FINAL rejection of all of the pending claims 1, 2, 4, 5, 7-16, and 18-20 in the Office Action dated 29 September 2003, and in support of the "Notice of Appeal" filed on 29 December 2003, Applicants hereby submit this Appeal Brief.

REAL PARTY IN INTEREST

Samsung Electronics Co., Ltd. owns all of the rights in the above-identified U.S. patent application by virtue of an Assignment executed by the inventors on 7 and

14 June 1999 and recorded by the Assignment Division of the U.S. Patent and Trademark Office on 4 October 2001 at Reel 010039, Frame 0446.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences related to this application or to any related application, nor will the disposition of this case affect, or be affected by, any other application directly or indirectly.

STATUS OF CLAIMS

Claims 1, 2, 4, 5, 7-16 and 18-20 remain pending. Claims 1, 2, 4, 5, 7-16 and 18-20 all stand rejected.

Accordingly, the claims on Appeal are claims 1, 2, 4, 5, 7-16 and 18-20.

STATUS OF AMENDMENTS

There are no pending Amendments with respect to this case.

SUMMARY OF INVENTION

The present invention is directed to a method of manufacturing a capacitor of a semiconductor device having a dielectric layer with a high dielectric constant.

As broadly recited in claim 1, the method comprises: forming a storage electrode (11a, FIG. 4) over a semiconductor substrate (1 - FIG. 4) (step 115 in FIGs.

5, 6, 7 and 8; page 8, lines 12-13); forming a high dielectric layer (15 - FIG. 4) over the storage electrode (step 120 in FIGs. 5, 6, 7 and 8; page 8, lines 14-17); forming a plate electrode (17 - FIG. 4) directly on the high dielectric layer (step 130 in FIG. 5; step 140 in FIG. 6; step 155 in FIG. 7; step 175 in FIG. 8; page 9, lines 19-21; page 10, lines 20-21; page 14, lines 19-20); performing a first post-annealing of the semiconductor substrate (step 125 in FIG. 5; step 145 in FIG. 6; step 165 in FIG. 7; step 170 in FIG. 8) under an inert atmosphere at a first temperature (page 9, lines 3-7; page 11, lines 8-11; page 13, lines 7-11; page 14, lines 13-18); and performing a second post-annealing of the semiconductor substrate (step 125 in FIG. 5; step 145 in FIG. 6; step 165 in FIG. 7; step 180 in FIG. 8), after the first post-annealing, at a second temperature lower than the first temperature in an oxygen environment (page 9, lines 7-9; page 11, lines 8-11; page 13, lines 7-11; page 15, lines 3-7), the first and second post-annealings being performed in-situ (page 9, lines 11-12; page 11, lines 15-16; etc.), wherein the plate electrode is formed of one selected from the group consisting of Pt, Ru, Ir, IrO_2, RuO_2, $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, and an alloy containing Ir (page 10, lines 1-3; page 11, line 1-3; etc.).

As broadly recited in claims 2 and 16, the high dielectric layer is formed of one selected from the group consisting of (Sr, Ti)O_3, (Ba, Sr)TiO_3, Pb(Zr, Ti)O_3 and (Pb, La)(ZrTi)O_3 (page 8, lines 17-19; page 10, lines 16-19; etc.).

As broadly recited in claims 4 and 18, the first temperature is between 600°C

and 900°C (page 9, line 4; page 11, line 9; etc.).

As broadly recited in claims 5 and 19, the second temperature is between 100°C and 600°C (page 9, line 9; page 11, line 13; etc.).

As broadly recited in claim 7, the post-annealing at the first and second temperatures are performed in a furnace or a rapid vacuum thermal annealing apparatus (page 9, lines 4-11; page 11, lines 9-15; etc.).

As broadly recited in claim 8, the first and second post-annealing steps are performed after the step of forming the high dielectric layer (FIGs. 5-8; page 9, lines 1-9; page 10, lines 12-14; etc.).

As broadly recited in claim 9, the method comprises: forming a storage electrode (11a - FIG. 4) over a semiconductor substrate (1 - FIG. 4) (step 115 in FIGs. 6 and 7; page 8, lines 12-13; page 10, lines 14-16; page 12, lines 11-13, 19-21); forming a high dielectric layer (15 - FIG. 4) over the storage electrode (step 120 in FIGs. 6 and 7; page 8, lines 14-17; page 10, lines 14-16; page 12, lines 11-13, 17-19); forming a plate electrode (17 - FIG. 4) directly on the high dielectric layer (step 140 in FIG. 6; step 155 in FIG. 7; page 9, lines 19-21; page 10, lines 14-16, 20-21; page 12, lines 11-13, 19-21); performing a first post-annealing of the semiconductor substrate (step 145 in FIG. 6; step 165 in FIG. 7) under an inert atmosphere at a first temperature (page 13, lines 7-11; page 14, lines 13-18); and performing a second post-annealing of the semiconductor substrate (step 145 in FIG. 6; step 165 in FIG. 7), after the first post-annealing, at a second temperature lower than the first

temperature in an oxygen environment (page 13, lines 7-11; page 15, lines 3-7), the first and second post-annealings being performed after the forming of the plate electrode (FIGs. 6 and 7; page 10, lines 12-14; page 12, lines 11-13), wherein the plate electrode is formed of one selected from the group consisting of Pt, Ru, Ir, IrO_2, RuO_2, $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, and an alloy containing Ir (page 11, line 1-3; page 12, lines 19-21).

As broadly recited in claims 10 and 13, the first post-annealing step is performed after the step of forming the high dielectric layer and the second post-annealing step is performed after the step of forming the plate electrode (FIGs. 6, 7 and 8; page 10, lines 12-14; page 12, lines 11-13; page 14, lines 7-10).

As broadly recited in claim 11, the method further comprises forming an interdielectric layer (19- FIG. 4) over the plate electrode (step 135 in FIG. 5; step 150 in FIG. 6; step 160 in FIG. 7; step 185 in FIG. 8; page 10, lines 4-5; page 12, lines 3-5; page 13, lines 3-5; page 15, lines 17-18).

As broadly recited in claim 12, the method comprises: forming a storage electrode (11a, FIG. 4) over a semiconductor substrate (1 - FIG. 4) (step 115 in FIG. 7; page 8, lines 12-13; page 12, lines 11-13, 19-21); forming a high dielectric layer (15 - FIG. 4) over the storage electrode (step 120 in FIG. 7; page 8, lines 14-17; page 12, lines 11-13, 17-19); forming a plate electrode (17 - FIG. 4) directly on the high dielectric layer (step 155 in FIG. 7; page 9, lines 19-21; page 12, lines 11-13, 19-21); performing a first post-annealing of the semiconductor substrate (step 165 in FIG. 7)

under an inert atmosphere at a first temperature (page 14, lines 13-18); and performing a second post-annealing of the semiconductor substrate (step 165 in FIG. 7), after the first post-annealing, at a second temperature lower than the first temperature in an oxygen environment (page 15, lines 3-7), forming an interdielectric layer over the plate electrode (step 160, FIG. 7); the first and second post-annealings being performed after the forming of the interdielectric layer (FIG. 7; page 12, lines 11-13), wherein the plate electrode is formed of one selected from the group consisting of Pt, Ru, Ir, IrO_2, RuO_2, $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, and an alloy containing Ir (page 11, line 1-3; page 12, lines 19-21).

As broadly recited in claims 14 and 20, performing a third post-annealing (step 125 in FIG. 5; step 145 in FIG. 6; etc.), after the second post annealing, at a temperature lower than the second temperature (page 9, lines 13-18; page 11, line 17 - page 12, line 2; etc.).

As broadly recited in claim 15, a method for manufacturing a capacitor of a semiconductor device in which: a storage electrode (11a - FIG. 4); a high dielectric layer (15 - FIG. 4); a plate electrode (17 - FIG. 4) formed directly on the high dielectric layer and comprising one selected from the group consisting of Pt, Ru, Ir, IrO_2, RuO_2, $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, and an alloy containing Ir (page 10, lines 1-3; page 11, line 1-3; etc.); and an interdielectric layer (19 - FIG. 4) are sequentially formed on a semiconductor

substrate (1 - FIG. 4), further comprising: performing a first post-annealing of the semiconductor substrate (step 145 in FIG. 6; step 165 in FIG. 7) under an inert atmosphere at a first temperature (page 13, lines 7-11; page 14, lines 13-18); and performing a second post-annealing of the semiconductor substrate, (step 145 in FIG. 6; step 165 in FIG. 7), after the first post-annealing, at a second temperature lower than the first temperature in an oxygen environment (page 13, lines 7-11; page 15, lines 3-7), the first and second post-annealings being performed after forming of the plate electrode (FIGs. 6 and 7; page 10, lines 12-14; page 12, lines 11-13).

ISSUES

The issues on Appeal are:

(I) whether claim 9 is patentable under 35 U.S.C. § 102 over Watanabe et al. U.S. Patent 5,439,845 ("Watanabe")

(II) whether claims 1-2, 4-5, 7-8 and 10 are patentable over Watanabe in combination with Ping et al. U.S. Patent 5,882,979 ("Ping");

(III) whether claims 11-16 and 18-20 are patentable over Watanabe in combination with Ping, Al-Shareef et al. U.S. Patent 6,162,744 (Al-Shareef") and Wolf Vol. 1, pp. 57, 183 and 388-9 ("Wolf").

GROUPING OF CLAIMS

Applicants respectfully assert that specifically, and for the purposes of this

Appeal only, the claims do not all stand or fall together. Specifically, and for the purposes of this Appeal only, Applicants deem claims 1, 2, 4, 5, 7, 8 and 10 to stand or fall together; claim 9 to stand or fall alone; claims 11 and 13 to stand or fall together; claim 12 to stand or fall alone; claim 14 to stand or fall alone; claims 15, 16, 18, and 19 to stand or fall together; and claim 20 to stand or fall alone.

ARGUMENTS

Issue I: Claim 9 Is Patentable Over Watanabe

In the FINAL Office Action dated 29 September 2003, the Examiner rejected claim 9 under 35 U.S.C. § 102 as allegedly being unpatentable over Watanabe.

Among other things, the method of claim 9 includes performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature; and performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature in an oxygen environment, the first and second post-annealings being performed after the forming of the plate electrode.

Applicants respectfully submit that Watanabe does not disclose any method including such a combination of features.

Watanabe discloses only two annealing steps "after the forming of the plate

electrode" - second anneal (1) (step 94) and second anneal (2) (step 96).[1] Watanabe does not disclose that the second anneal (2) (step 96) is performed "at a second temperature lower than the first temperature" at which the second anneal (1) (step 94) is performed. Indeed, col. 15, lines 12-14 clearly state that "[t]he second anneal is preferably performed in an electric furnace at **a** temperature . . . ." Thus, Watanabe teaches that the second anneal (which includes both steps 94 and 96) is performed at **a** (singular) temperature. This is in direct contrast to the method of claim 9 where the second post-annealing (e.g., step 96 of Watanabe) is performed at a temperature that is lower than the temperature at which the first post-annealing (e.g., step 94 of Watanabe) is performed.

Therefore, the second anneal (1) (step 94) and second anneal (2) (step 96) of Watanabe cannot correspond to the first and second post-annealings of claim 9.

So, for at least this reason, Applicants respectfully submit that claim 9 is clearly patentable over Watanabe under 35 U.S.C. § 102.

Furthermore, as noted above, the first and second post-annealings of claim 9 are performed in completely different environments. The first post-annealing of claim 9 is performed in an oxygen environment, while the second post-annealing of claim 9 is performed in an inert environment.

Watanabe does not disclose that the second anneal (2) (step 96) is performed in

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[1] Watanabe clearly discloses that the annealing step 92 is performed before forming the plate electrode, and therefore it cannot correspond to any of the post-annealing steps of claim 9 (see FIG. 1).

a different environment than that at which the second anneal (1) (step 94) is performed. Indeed, Watanabe teaches that the second anneal (which comprises both steps 94 and 96) should be performed in an oxygen environment (see col. 15, lines 35-39).

Accordingly, for the foregoing reasons, Applicants respectfully submit that claim 9 is patentable over Watanabe.

Issue II: Claims 1-2, 4-5, 7-8 and 10 Are Patentable Over Watanabe in Combination with Ping

Claim 1

Among other things, the method of claim 1 includes performing a **first post-annealing** of the semiconductor substrate under an **inert atmosphere** at a first temperature; and performing a **second post-annealing** of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature in an **oxygen environment**, the first and second post-annealings being performed in-situ.

At the outset, in rejecting claim 1, the Office Action fails to mention the first post-annealing being performed under an **inert atmosphere** or the second post-annealing being performed in an **oxygen environment**.

Applicants respectfully submit that neither Watanabe nor Ping, nor any combination thereof discloses or suggests any method including this combination of

features.

Watanabe discloses a total of three annealing steps - first anneal (step 92), second anneal (1) (step 94) and second anneal (2) (step 96). Watanabe clearly teaches that first anneal (step 92) is performed in an oxygen environment (see col. 14, lines 37-41). Therefore, Watanabe's first anneal (step 92) cannot correspond to the recited **first post-annealing** of the semiconductor substrate under an **inert atmosphere**.

So, that only leaves the second anneal (1) (step 94) and second anneal (2) (step 96) as candidates to correspond to the first and second post-annealing steps recited in claim 1.

However, Watanabe does not disclose that the second anneal (2) (step 96) is performed "at a second temperature lower than the first temperature" at which the second anneal (1) (step 94) is performed. Indeed, col. 15, lines 12-14 clearly state that "[t]he second anneal is preferably performed in an electric furnace at **a** temperature . . . ." Thus, Watanabe teaches that the second anneal (which includes both steps 94 and 96) is performed at **a** (singular) temperature. This is in direct contrast to the method of claim 9 where the second post-annealing (e.g., step 96 of Watanabe) is performed at a temperature that is lower than the temperature at which the first post-annealing (e.g., step 94 of Watanabe) is performed.

Therefore, the second anneal (1) (step 94) and second anneal (2) (step 96) of Watanabe cannot correspond to the first and second post-annealings of claim 1.

Ping, which has been cited only for showing various processes being

performed *in-situ*, does not remedy this shortcoming of Watanabe.

So, for at least this reason, Applicants respectfully submit that claim 1 is clearly patentable over any possible combination of Watanabe and Ping under 35 U.S.C. § 103.

Furthermore, as noted above, the first and second post-annealings of claim 1 are performed in completely different environments. The first post-annealing of claim 1 is performed in an oxygen environment, while the second post-annealing of claim 1 is performed in an inert environment.

Watanabe does not disclose that the second anneal (2) (step 96) is performed in a different environment than that at which the second anneal (1) (step 94) is performed. Indeed, Watanabe teaches that the second anneal (which comprises both steps 94 and 96) should be performed in an oxygen environment (see col. 15, lines 35-39).

So, for at least this additional reason, Applicants respectfully submit that claim 1 is clearly patentable over any possible combination of Watanabe and Ping under 35 U.S.C. § 103.

Finally, neither Watanabe and Ping disclose performing two annealing processes under two very different environments (inert environment, and oxygen environment) *in situ*. So no combination of Watanabe and Ping could produce the method of claim 1.

Moreover, to the extent that the Examiner is taking "Official Notice" that it

was a common practice **at the time of Applicants' invention** to perform two annealing processes under two very different environments (inert environment, and oxygen environment) *in situ*, as recited in claim 1, Applicants respectfully traverse the "Official Notice" and request that the Examiner provide specific evidence in support of the specific facts of which Official Notice is supposedly being taken.[2]

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that claim 1 is patentable under 35 U.S.C. § 103 over any combination of Watanabe and Ping.

Claims 2, 4, 5, 7, 8, and 10

Claims 2, 4, 5, 7, 8 and 10 depend from claim 1 and are deemed patentable over Watanabe and Ping for at least the reasons set forth above with respect to claim 1.

Issue III. Claims 11-16 and 18-20 Are Patentable Over Watanabe in Combination with Ping, Al-Shareef, and Wolf

Claim 11

Claim 11 depends from claim 1. As explained in detail below, Applicants respectfully submit that Al-Shareef and Wolf do not remedy the shortcomings of Watanabe and Ping with respect to claim 1 and accordingly, claim 11 is deemed

[2] The Examiner asserts at the top of page 4 that "it **is** well known and commonly practiced . . . ." Of course the test under 35 U.S.C. § 103 is **not** what "is" known today, but what "was" known **at the time of Applicant's invention**!

patentable over any combination of Watanabe, Ping, Al-Shareef and Wolf.

More specifically, like Watanabe and Ping, Al-Shareef and Wolf, alone or in combination, fail to disclose or suggest performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature; and performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature in an oxygen environment, the first and second post-annealings being performed after the forming of the plate electrode.

Indeed, Al-Shareef specifically **teaches away** from the claimed method, teaching that the annealings are to be conducted "*prior to formation of ANY portion of the second capacitor electrode 32*" to minimize the risk of oxidation of the plate electrode 32 due to out-diffusion of oxygen from the high dielectric layer 26 (col. 5, lines 6-11). This was especially critical for Al-Shareef in so much as it teaches that the plate electrode is a polysilicon layer, not a noble-metal-based material as in the invention of claim 11.

M.P.E.P. § 2141.02 states that "PRIOR ART MUST BE CONSIDERED IN ITS ENTIRETY, INCLUDING DISCLOSURES THAT TEACH AWAY FROM THE CLAIMS" (emphasis in original text). For example, it was held that a reference teaching that a PTFE material should be stretched slowly **taught away from** a claimed process that included a step of rapidly stretching the PTFE material (M.P.E.P. § 2141.02 citing W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220

USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984)). So, in that case, the reference "anticipated performing [a rapid stretching of the PTFE material], but concluded that such a strategy was undesirable for the reasons disclosed by the reference" (paraphrasing the Office Action). However, the courts concluded that the reference taught away from the claimed process and could not be used - or even combined with any other reference (see M.P.E.P. § 2145 - "*it is improper to combine references where the references teach away from their combination*") - to produce the claimed invention.

Applicants respectfully submit that this is exactly the same case here with respect to Al-Shareef.

Meanwhile, Wolf merely teaches that some kinds of anneals may be performed during fabrication of a VLSI device. Wolf does not appear to teach anything specifically about a process for forming a capacitor. Wolf does not disclose any process of forming a capacitor that includes performing the recited first and second annealings under the specifically recited conditions of claim 11 (performing a **first post-annealing** of the semiconductor substrate under an **inert atmosphere** at a first temperature; and performing a **second post-annealing** of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature in an **oxygen environment**). Nor, as explained above, can it be combined with Al-Shareef that teaches away from the method of claim 11.

Accordingly, Applicants respectfully submit that no possible combination of

Watanabe, Ping, Al-Shareef and Wolf could possibly produce the method of claim 11.

Furthermore, the Examiner has provided no citation to anything in the prior art that supports any of the various alleged motivations to combine the references that are given in paragraph 9, lines 6-17 ("to provide a flat, low resistance interconnect;" "to reduce the post capacitor thermal budget;" "to reduce the risk of oxidation of either of the electrodes from any out-diffusion of oxygen from the high dielectric layer;" etc.).

The Examiner has taken "Official Notice" that "it is well known in the art to form an interdielectric layer and that various essential thermal interconnect processes, or anneals, are commonly performed throughout the industry, after the formation of the capacitor plate and the interdielectric layer."[3]

Of course, none of that is what Applicants have specifically claimed in claim 11! Applicants have not claimed annealing in general, forming interdielectric layers in general, etc. Applicants have claimed a very specific process performed under very specific conditions. Applicants fail to understand the significance of anything of which the Examiner has taken "Official Notice" with respect to the actual subject matter of Applicants' claim 11.

Also, to the extent that the Examiner is taking "Official Notice" that any of the actually recited features of claim 11 were well-known or commonly practiced **at the time of Applicants' invention**, Applicants respectfully traverse the "Official Notice"

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[3] The Examiner asserts on page 5 that "it **is** well known in the art to form an interdielectric layer and . . . ." Of course the test under 35 U.S.C. § 103 is **not** what "is" known today, but what "was" known **at the time of Applicant's invention**!

and request that the Examiner provide specific evidence in support of the specific facts of which "Official Notice" is supposedly being taken.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that claim 11 is patentable under 35 U.S.C. § 103 over any combination of Watanabe, Ping, Al-Shareef and Wolf.

Claim 12

Among other things, the method of claim 12 includes performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature; performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature in an oxygen environment; and forming an interdielectric layer over the plate electrode, the first and second post-annealings being performed after the forming of the interdielectric layer.

Applicants respectfully submit that neither Watanabe, Ping, Al-Shareef, nor Wolf, nor any combination thereof, discloses or suggests any method including this combination of features.

As explained above with respect to claim 1, Watanabe does not disclose that the second anneal (2) (step 96) is performed "at a second temperature lower than the first temperature" at which the second anneal (1) (step 94) is performed, and Ping does not remedy that shortcoming. Furthermore, as explained above with respect to claim 11, Al-Shareef specifically **teaches away** from the claimed method, teaching

that the annealings are to be conducted "*prior to formation of ANY portion of the second capacitor electrode 32*" and therefore, necessarily, before the forming of the interdielectric layer. Finally, as also explained above with respect to claim 11, Wolf does not even appear to teach anything specifically about a process for forming a capacitor at all! Wolf does not disclose any process of forming a capacitor that includes performing a **first post-annealing** of the semiconductor substrate under an **inert atmosphere** at a first temperature; and performing a **second post-annealing** of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature in an **oxygen environment**.

Accordingly, Applicants respectfully submit that no possible combination of Watanabe, Ping, Al-Shareef and Wolf could possibly produce the method of claim 12.

Furthermore, the Examiner has provided no citation to anything in the prior art that supports any of the various alleged motivations to combine the references that are given in paragraph 9, lines 6-17 ("to provide a flat, low resistance interconnect;" "to reduce the post capacitor thermal budget;" "to reduce the risk of oxidation of either of the electrodes from any out-diffusion of oxygen from the high dielectric layer;" etc.).

The Examiner has taken "Official Notice" that "it is well known in the art to form an interdielectric layer and that various essential thermal interconnect processes, or anneals, are commonly performed throughout the industry, after the formation of

the capacitor plate and the interdielectric layer."[4]

Of course, none of that is what Applicants have specifically claimed in claim 12! Applicants have not claimed annealing in general, forming interdielectric layers in general, etc. Applicants have claimed a very specific process performed under very specific conditions. Applicants fail to understand the significance of anything of which the Examiner has taken "Official Notice" with respect to the actual subject matter of Applicants' claim 12.

Also, to the extent that the Examiner is taking "Official Notice" that any of the actually recited features of claim 12 were well-known or commonly practiced **at the time of Applicants' invention**, Applicants respectfully traverse the "Official Notice" and request that the Examiner provide specific evidence in support of the specific facts of which "Official Notice" is supposedly being taken.

Accordingly, for the foregoing reasons, Applicants respectfully submit that claim 12 is patentable under 35 U.S.C. § 103 over any combination of Watanabe, Ping, Al-Shareef and Wolf.

Claim 13

Claim 13 depends from claim 11 and is deemed patentable over Watanabe, Ping, Al-Shareef and Wolf for at least the reasons set forth above with respect to claim 11.

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[4] The Examiner asserts on page 5 that "it **is** well known in the art to form an interdielectric layer and . . . ." Of course the test under 35 U.S.C. § 103 is **not** what "is" known today, but what "was" known **at the time of Applicant's invention**!

Claim 14

Claim 14 depends from claim 1. As explained above with respect to claim 11, Applicants respectfully submit that Al-Shareef and Wolf do not remedy the shortcomings of Watanabe and Ping with respect to claim 1 and accordingly, claim 14 is deemed patentable over any combination of Watanabe, Ping, Al-Shareef and Wolf for at least the reasons set forth above with respect to claim 1, and for the following additional reasons.

Among other things, the method of claim 14 includes performing a third post-annealing, after the second post annealing, **at a temperature lower than the second temperature**.

Applicants respectfully submit that no method including this feature is disclosed or suggested by Watanabe, Ping, Al-Shareef or Wolf or any combination thereof.

The Examiner has failed to cite any text or Figure in any of the references where such a feature is supposedly disclosed in the context of a method having the features of claim 1. Instead, the Examiner has simply stated that "It would be obvious to one of ordinary skill in the art to perform a third anneal at a lower temperature in order to reduce oxygen vacancy and densify the film."

Applicants respectfully traverse this conclusory statement, and respectfully note that the Examiner has not provided any citation in support thereof. It is well established that such conclusory statements, unsupported by any facts or citations,

cannot meet the Examiner's burden under 35 U.S.C. § 103. See In re Lee 61 USPQ2d 1430, 1434 ("the examiner can satisfy the burden of showing obviousness of the combination only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead the individual to combine the relevant teachings of the references") (emphasis added).

Also, Applicants respectfully submit that St Regis Paper Co., cited in the Office Action, is not on point. First, the Examiner has failed to cite any prior art that discloses the claimed method, except including some "single step" that the Examiner is alleging that Applicants have divided into multiple steps. So the predicate for St Regis Paper Co., has not even been established here. Furthermore, Applicants respectfully submit that they have not divided any "single step" into multiple steps. Applicants have claimed a method on claim 14 which has three different annealing steps performed under three different sets of conditions. There is no way to somehow "combine' these steps performed under different process conditions into some hypothetical "single step."

Meanwhile, the Examiner has taken "Official Notice" that "it is well known in the art to form an interdielectric layer and that various essential thermal interconnect processes, or anneals, are commonly performed throughout the industry, after the formation of the capacitor plate and the interdielectric layer."[5]

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[5] The Examiner asserts on page 5 that "it **is** well known in the art to form an interdielectric layer and . . . ." Of course the test under 35 U.S.C. § 103 is **not** what "is" known today, but what "was" known **at the time of Applicant's invention**!

Of course, none of that is what Applicants have specifically claimed in claim 14! Applicants have not claimed annealing in general, forming interdielectric layers in general, etc. Applicants have claimed a very specific process performed under very specific conditions. Applicants fail to understand the significance of anything of which the Examiner has taken "Official Notice" with respect to the actual subject matter of Applicants' claim 14.

Also, to the extent that the Examiner is taking "Official Notice" that any of the actually recited features of claim 14 were well-known or commonly practiced **at the time of Applicants' invention**, Applicants respectfully traverse the "Official Notice" and request that the Examiner provide specific evidence in support of the specific facts of which "Official Notice" is supposedly being taken.

Accordingly, for at least these additional reasons, Applicants respectfully submit that claim 14 is patentable under 35 U.S.C. § 103 over any combination of Watanabe, Ping, Al-Shareef and Wolf.

Claim 15

Among other things, the method of claim 15 includes performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature; and performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature in an oxygen environment, the first and second post-annealings being performed after forming of the plate electrode.

As explained above with respect to claim 1, Watanabe does not disclose that the second anneal (2) (step 96) is performed "at a second temperature lower than the first temperature" at which the second anneal (1) (step 94) is performed, and Ping does not remedy that shortcoming. Furthermore, as explained above with respect to claim 11, Al-Shareef specifically **teaches away** from the claimed method, teaching that the annealings are to be conducted "*prior to formation of ANY portion of the second capacitor electrode 32*" and therefore, necessarily, before the forming of the interdielectric layer. Finally, as also explained above with respect to claim 11, Wolf Wolf does not even appear to teach anything specifically about a process for forming a capacitor at all! Wolf does not disclose any process of forming a capacitor that includes performing a **first post-annealing** of the semiconductor substrate under an **inert atmosphere** at a first temperature; and performing a **second post-annealing** of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature in an **oxygen environment**.

Accordingly, Applicants respectfully submit that no possible combination of Watanabe, Ping, Al-Shareef and Wolf could possibly produce the method of claim 15.

Furthermore, the Examiner has provided no citation to anything in the prior art that supports any of the various alleged motivations to combine the references that are given in paragraph 9, lines 6-17 ("to provide a flat, low resistance interconnect;" "to reduce the post capacitor thermal budget;" "to reduce the risk of oxidation of either of the electrodes from any out-diffusion of oxygen from the high dielectric layer;" etc.).

The Examiner has taken "Official Notice" that "it is well known in the art to form an interdielectric layer and that various essential thermal interconnect processes, or anneals, are commonly performed throughout the industry, after the formation of the capacitor plate and the interdielectric layer."[6]

Of course, none of that is what Applicants have specifically claimed in claim 15! Applicants have not claimed annealing in general, forming interdielectric layers in general, etc. Applicants have claimed a very specific process performed under very specific conditions. Applicants fail to understand the significance of anything of which the Examiner has taken "Official Notice" with respect to the actual subject matter of Applicants' claim 15.

Also, to the extent that the Examiner is taking "Official Notice" that any of the actually recited features of claim 15 were well-known or commonly practiced **at the time of Applicants' invention**, Applicants respectfully traverse the "Official Notice" and request that the Examiner provide specific evidence in support of the specific facts of which "Official Notice" is supposedly being taken.

Accordingly, for the foregoing reasons, Applicants respectfully submit that claim 15 is patentable under 35 U.S.C. § 103 over any combination of Watanabe, Ping, Al-Shareef and Wolf.

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[6] The Examiner asserts on page 5 that "it **is** well known in the art to form an interdielectric layer and . . . ." Of course the test under 35 U.S.C. § 103 is **not** what "is" known today, but what "was" known **at the time of Applicant's invention**!

Claims 16 and 18-19

Claims 16 and 18-19 depend from claim 15 and are deemed allowable for at least the reasons set forth above with respect to claim 15.

Claim 20

Claim 20 depends from claim 15 and is deemed allowable for at least the reasons set forth above with respect to claim 15, and for the following additional reasons.

Among other things, the method of claim 15 includes performing a third post-annealing, after the second post annealing, **at a temperature lower than the second temperature**.

For all the reasons given above with respect to claim 14, Applicants respectfully submit that no method including this feature is disclosed or suggested by Watanabe, Ping, Al-Shareef or Wolf or any combination thereof.

Also, to the extent that the Examiner is taking "Official Notice" that any of the actually recited features of claim 20 were well-known or commonly practiced **at the time of Applicants' invention**, Applicants respectfully traverse the "Official Notice" and request that the Examiner provide specific evidence in support of the specific facts of which "Official Notice" is supposedly being taken.

Accordingly, for at least these additional reasons, Applicants respectfully submit that claim 20 is patentable under 35 U.S.C. § 103 over any combination of Watanabe, Ping, Al-Shareef and Wolf.

CONCLUSION

For all of the foregoing reasons, Applicants respectfully submit that claims 1, 2, 4, 5, 7-16 and 18-20 are each patentable over the cited prior art. Therefore, Applicants respectfully request that claims 1, 2, 4, 5, 7-16 and 18-20 be allowed and the application be passed to issue.

Respectfully submitted,

VOLENTINE FRANCOS, P.L.L.C.

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By: _____
Kenneth D. Springer
Registration No. 39,843

VOLENTINE FRANCOS, P.L.L.C.
12200 Sunrise Valley Drive, Suite 150
Reston, Virginia 20191
Telephone No.: (703) 715-0870
Facsimile No.: (703) 715-0877

APPENDIX - CLAIMS ON APPEAL

1. A method for manufacturing a capacitor of a semiconductor device, comprising:

forming a storage electrode over a semiconductor substrate;

forming a high dielectric layer over the storage electrode;

forming a plate electrode directly on the high dielectric layer;

performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature; and

performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature in an oxygen environment,

the first and second post-annealings being performed in-situ,

wherein the plate electrode is formed of one selected from the group consisting of Pt, Ru, Ir, IrO_2, RuO_2, $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, and an alloy containing Ir.

2. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the high dielectric layer is formed of one selected from the group consisting of (Sr, Ti)O_3, (Ba, Sr)TiO_3, Pb(Zr, Ti)O_3 and (Pb, La)(ZrTi)O_3.

4. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the first temperature is between 600°C and 900°C.

5. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the second temperature is between 100°C and 600°C.

7. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the post-annealing at the first and second temperatures are performed in a furnace or a rapid vacuum thermal annealing apparatus.

8. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the first and second post-annealing steps are performed after the step of forming the high dielectric layer.

9. A method for manufacturing a capacitor of a semiconductor device, comprising:

forming a storage electrode over a semiconductor substrate;

forming a high dielectric layer over the storage electrode;

forming a plate electrode directly on the high dielectric layer;

performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature; and

performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature in an oxygen environment,

the first and second post-annealings being performed after the forming of the plate electrode,

wherein the plate electrode is formed of one selected from the group consisting of Pt, Ru, Ir, IrO_2, RuO_2, $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, and an alloy containing Ir.

10. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the first post-annealing step is performed after the step of forming the high dielectric layer and the second post-annealing step is performed after the step of forming the plate electrode.

11. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, further comprising forming an interdielectric layer over the plate electrode.

12. A method for manufacturing a capacitor of a semiconductor device, comprising:

forming a storage electrode over a semiconductor substrate;

forming a high dielectric layer over the storage electrode;

forming a plate electrode directly on the high dielectric layer;

performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature;

performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature in an oxygen environment; and

forming an interdielectric layer over the plate electrode,

the first and second post-annealings being performed after the forming of the interdielectric layer,

wherein the plate electrode is formed of one selected from the group consisting of Pt, Ru, Ir, IrO_2, RuO_2, $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, and an alloy containing Ir.

13. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 11, wherein the first post-annealing step is performed after the step of forming the high dielectric layer and the second post-annealing step is performed after the step of forming the plate electrode.

14. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, further comprising performing a third post-annealing, after the second post annealing, at a temperature lower than the second temperature.

15. A method for manufacturing a capacitor of a semiconductor device in which: a storage electrode; a high dielectric layer; a plate electrode formed directly on the high dielectric layer and comprising one selected from the group consisting of Pt, Ru, Ir, IrO_2, RuO_2, $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, and an alloy containing Ir; and an interdielectric layer are sequentially formed on a semiconductor substrate, further comprising:

performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature; and

performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature in an oxygen environment,

the first and second post-annealings being performed after forming of the plate electrode.

16. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 15, wherein the high dielectric layer is formed of one selected from the group consisting of (Sr, Ti)O_3, (Ba, Sr)TiO_3, Pb(Zr, Ti)O_3 and (Pb, La)$(ZrTi)O_3$.

18. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 15, wherein the first temperature is between 600°C and 900°C.

19. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 15, wherein the second temperature is between 100°C and 600°C.

20. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 15, further comprising performing a third post-annealing, after the second post annealing, at a temperature lower than the second temperature.